

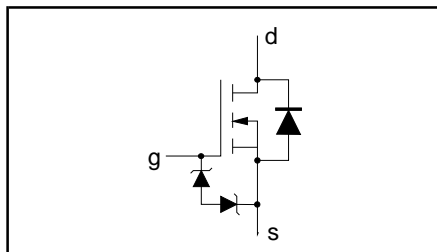
# TrenchMOS™ transistor Logic level FET

## PHP60N06LT, PHB60N06LT

### FEATURES

- 'Trench' technology
- Very low on-state resistance
- Fast switching
- Stable off-state characteristics
- High thermal cycling performance
- Low thermal resistance

### SYMBOL



### QUICK REFERENCE DATA

$V_{DSS} = 55 \text{ V}$
$I_D = 58 \text{ A}$
$R_{DS(ON)} \leq 20 \text{ m}\Omega (V_{GS} = 5 \text{ V})$
$R_{DS(ON)} \leq 18 \text{ m}\Omega (V_{GS} = 10 \text{ V})$

### GENERAL DESCRIPTION

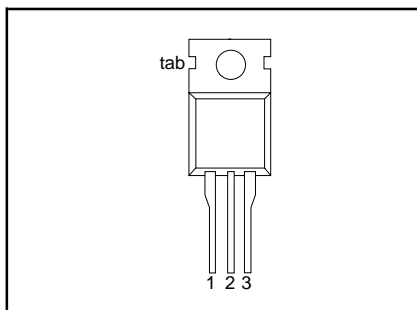
N-channel enhancement mode, logic level, field-effect power transistor in a plastic envelope using 'trench' technology. The device has very low on-state resistance. It is intended for use in dc to dc converters and general purpose switching applications.

The PHP60N06LT is supplied in the SOT78 (TO220AB) conventional leaded package.  
The PHB60N06LT is supplied in the SOT404 surface mounting package.

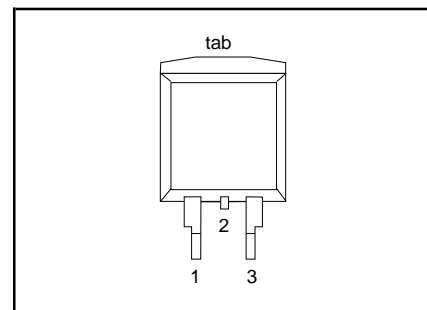
### PINNING

PIN	DESCRIPTION
1	gate
2	drain <sup>1</sup>
3	source
tab	drain

### SOT78 (TO220AB)



### SOT404



### LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DSS}$	Drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$	-	55	V
$V_{DGR}$	Drain-gate voltage	$T_j = 25 \text{ }^\circ\text{C}$ to $175 \text{ }^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	55	V
$V_{GS}$	Gate-source voltage		-	$\pm 13$	V
$I_D$	Continuous drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	58	A
		$T_{mb} = 100 \text{ }^\circ\text{C}$	-	40	A
$I_{DM}$	Pulsed drain current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	232	A
$P_D$	Total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	150	W
$T_j, T_{stg}$	Operating junction and storage temperature		- 55	175	$^\circ\text{C}$

<sup>1</sup> It is not possible to make connection to pin 2 of the SOT404 package.

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### THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	1.0	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	SOT78 package, in free air SOT404 package, pcb mounted, minimum footprint	60 50	- -	K/W K/W

### ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 k $\Omega$ )	-	2	kV

### ELECTRICAL CHARACTERISTICS

$T_j = 25^\circ\text{C}$  unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA};$ $T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{(BR)GSS}$	Gate-source breakdown voltage	$I_G = \pm 1\text{ mA};$	10	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$ $T_j = 175^\circ\text{C}$ $T_j = -55^\circ\text{C}$	1.0 0.5 -	1.5 -	2.0 - 2.3	V V V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}; I_D = 25\text{ A}$ $V_{GS} = 10\text{ V}; I_D = 25\text{ A}$ $T_j = 175^\circ\text{C}$	- - -	15 16	20 18 42	m $\Omega$ m $\Omega$ m $\Omega$
$g_{fs}$	Forward transconductance	$V_{DS} = 25\text{ V}; I_D = 25\text{ A}$	20	52	-	S
$I_{GSS}$	Gate source leakage current	$V_{GS} = \pm 5\text{ V}; V_{DS} = 0\text{ V}$ $T_j = 175^\circ\text{C}$	-	0.02	1	$\mu\text{A}$ $\mu\text{A}$
$I_{DSS}$	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V};$ $T_j = 175^\circ\text{C}$	-	0.05	10	$\mu\text{A}$ $\mu\text{A}$
$Q_{g(tot)}$	Total gate charge	$I_D = 50\text{ A}; V_{DD} = 44\text{ V}; V_{GS} = 5\text{ V}$	-	37	-	nC
$Q_{gs}$	Gate-source charge		-	10	-	nC
$Q_{gd}$	Gate-drain (Miller) charge		-	17	-	nC
$t_{don}$	Turn-on delay time	$V_{DD} = 30\text{ V}; I_D = 25\text{ A};$	-	28	40	ns
$t_r$	Turn-on rise time	$V_{GS} = 5\text{ V}; R_G = 10\ \Omega$	-	110	160	ns
$t_{doff}$	Turn-off delay time	Resistive load	-	95	135	ns
$t_f$	Turn-off fall time		-	70	90	ns
$L_d$	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
$L_d$	Internal drain inductance	Measured from drain lead to centre of die (SOT78 package only)	-	4.5	-	nH
$L_s$	Internal source inductance	Measured from source lead to source bond pad	-	7.5	-	nH
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	1800	2400	pF
$C_{oss}$	Output capacitance		-	350	420	pF
$C_{rss}$	Feedback capacitance		-	170	235	pF

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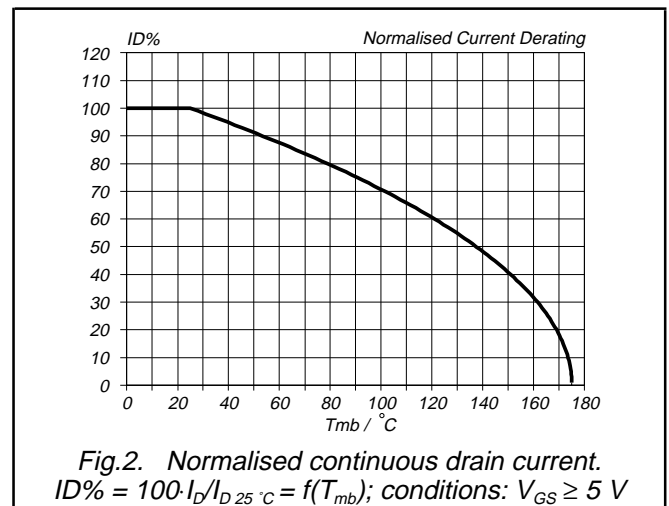
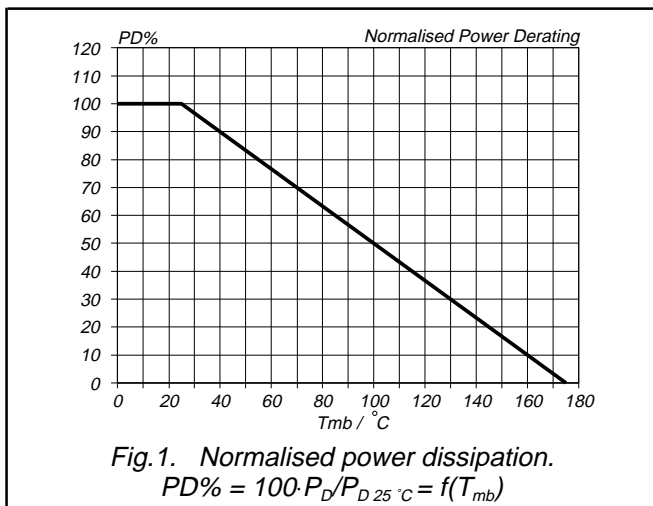
**REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS**

T<sub>j</sub> = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>S</sub>	Continuous source current (body diode)		-	-	58	A
I <sub>SM</sub>	Pulsed source current (body diode)		-	-	232	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V	-	0.95	1.2	V
		I <sub>F</sub> = 40 A; V <sub>GS</sub> = 0 V	-	1.0	-	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 40 A; -di <sub>F</sub> /dt = 100 A/μs;	-	47	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = -10 V; V <sub>R</sub> = 30 V	-	0.15	-	μC

**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W <sub>DSS</sub>	Drain-source non-repetitive unclamped inductive turn-off energy	I <sub>D</sub> = 45 A; V <sub>DD</sub> ≤ 25 V; V <sub>GS</sub> = 5 V; R <sub>GS</sub> = 50 Ω; T <sub>mb</sub> = 25 °C	-	110	mJ



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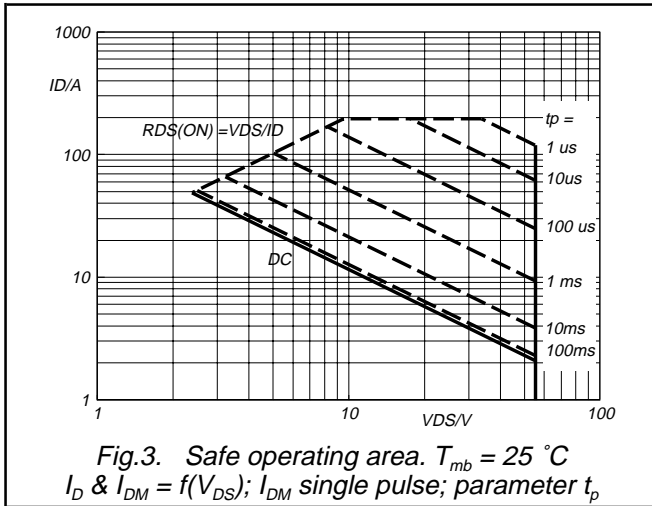


Fig.3. Safe operating area.  $T_{mb} = 25^\circ\text{C}$   
 $I_D$  &  $I_{DM} = f(V_{DS})$ ;  $I_{DM}$  single pulse; parameter  $t_p$

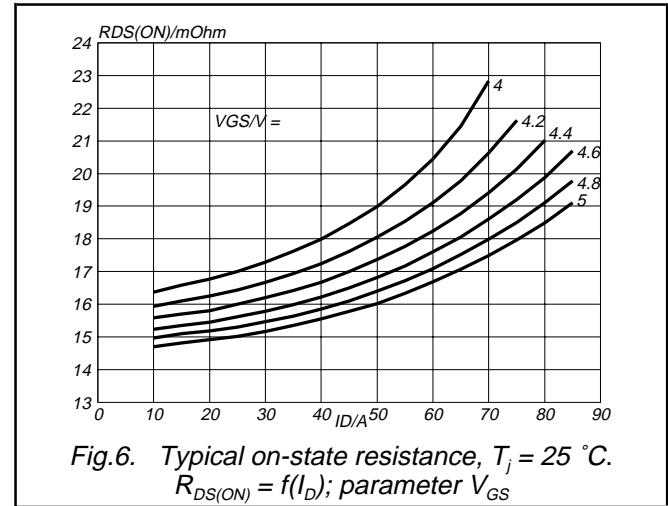


Fig.6. Typical on-state resistance,  $T_j = 25^\circ\text{C}$ .  
 $R_{DS(ON)} = f(I_D)$ ; parameter  $V_{GS}$

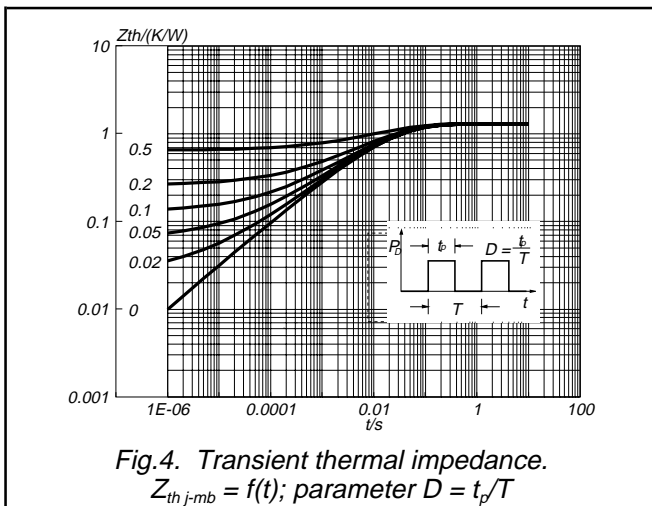


Fig.4. Transient thermal impedance.  
 $Z_{th-j-mb} = f(t)$ ; parameter  $D = t_p/T$

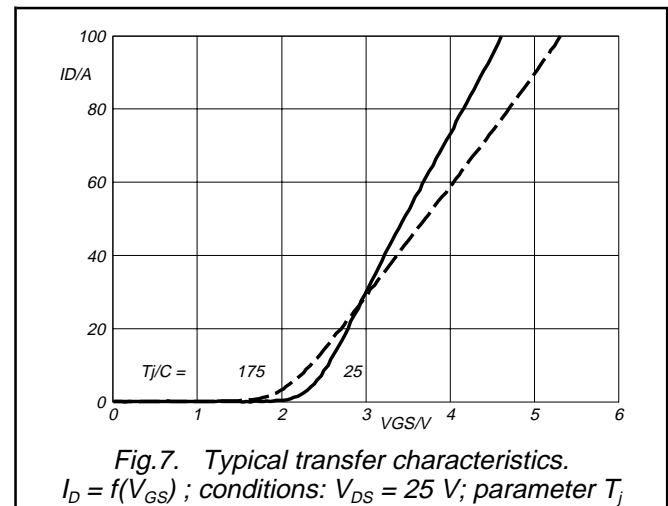


Fig.7. Typical transfer characteristics.  
 $I_D = f(V_{GS})$ ; conditions:  $V_{DS} = 25\text{ V}$ ; parameter  $T_j$

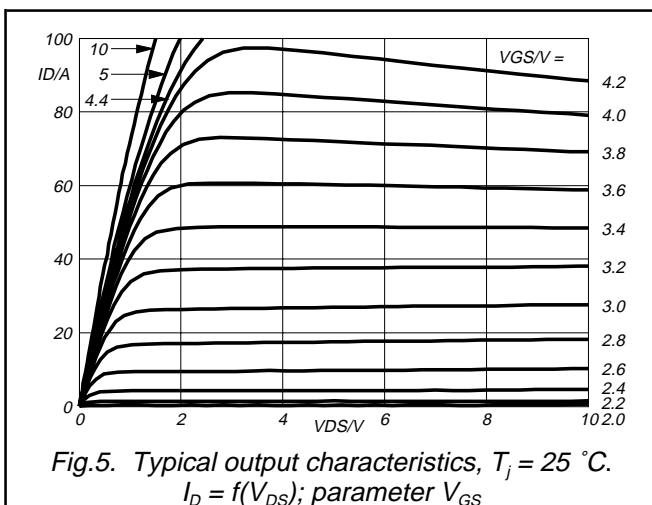


Fig.5. Typical output characteristics,  $T_j = 25^\circ\text{C}$ .  
 $I_D = f(V_{DS})$ ; parameter  $V_{GS}$

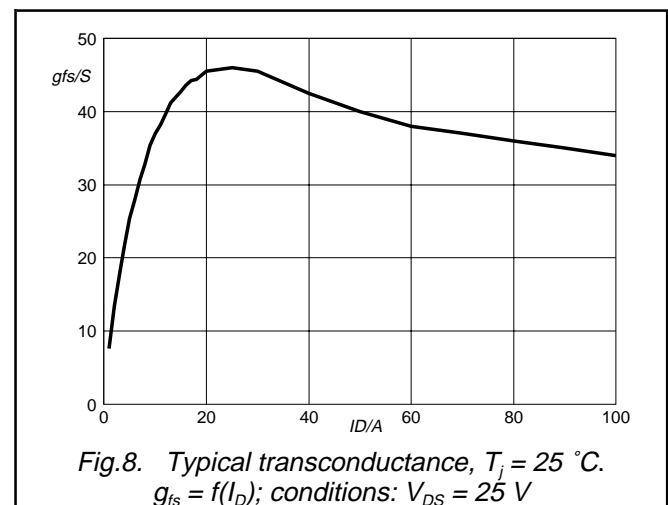
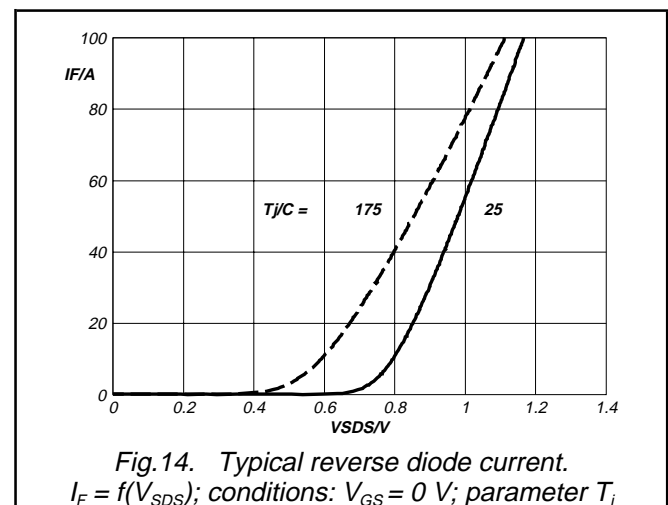
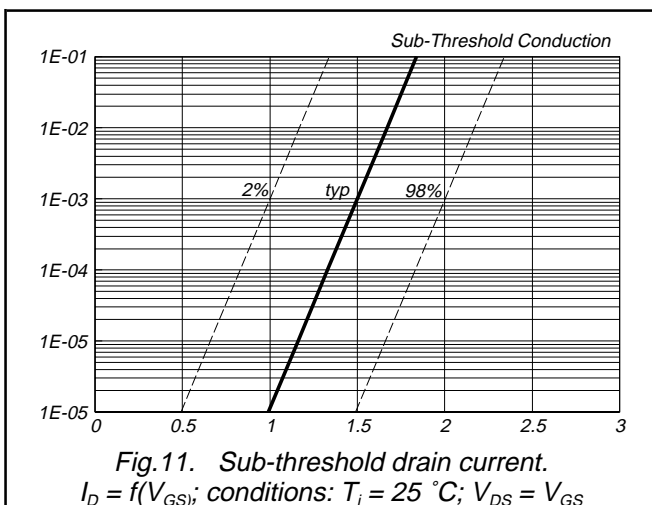
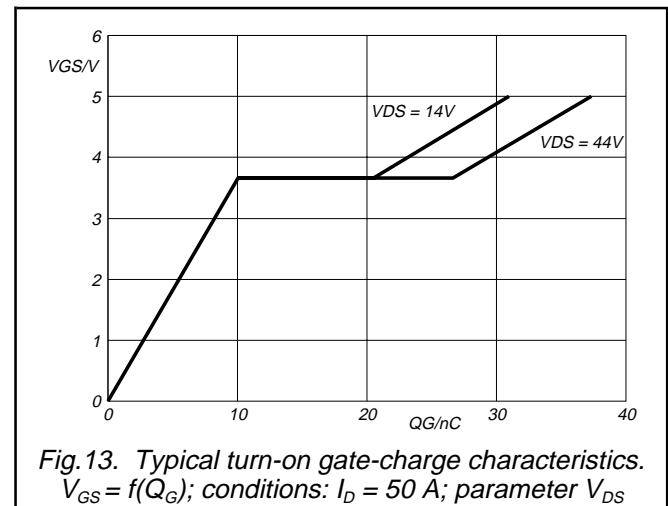
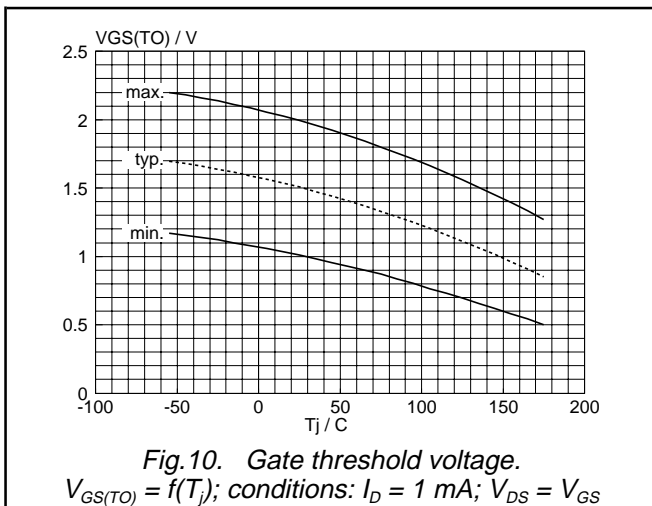
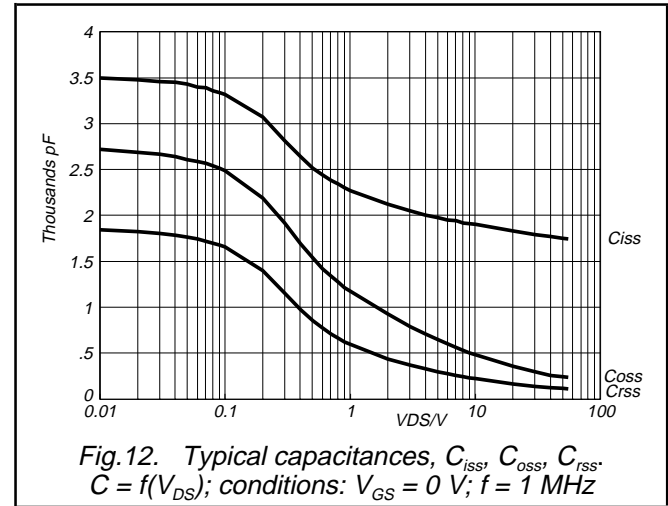
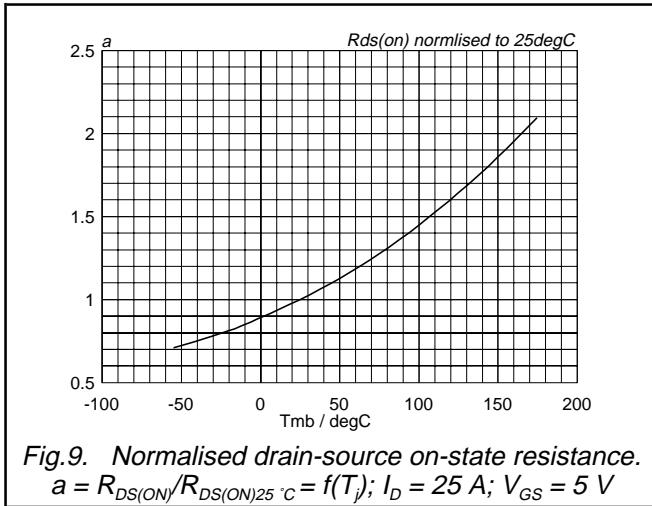


Fig.8. Typical transconductance,  $T_j = 25^\circ\text{C}$ .  
 $g_{fs} = f(I_D)$ ; conditions:  $V_{DS} = 25\text{ V}$

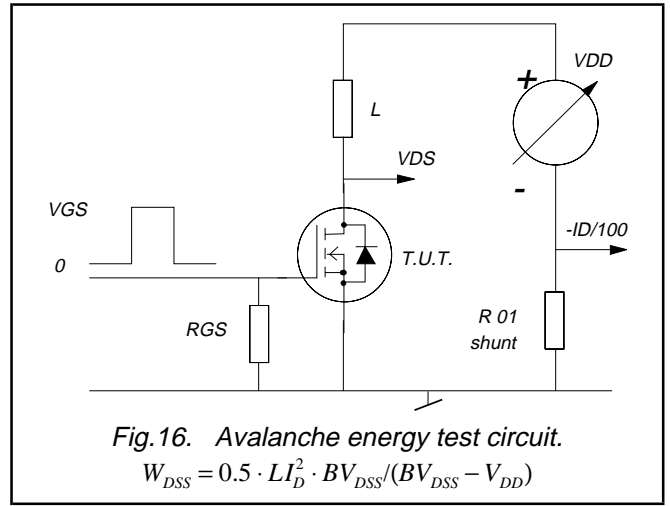
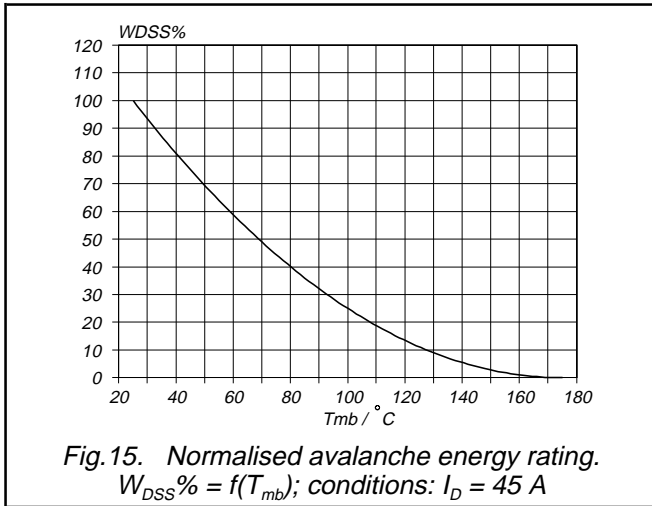
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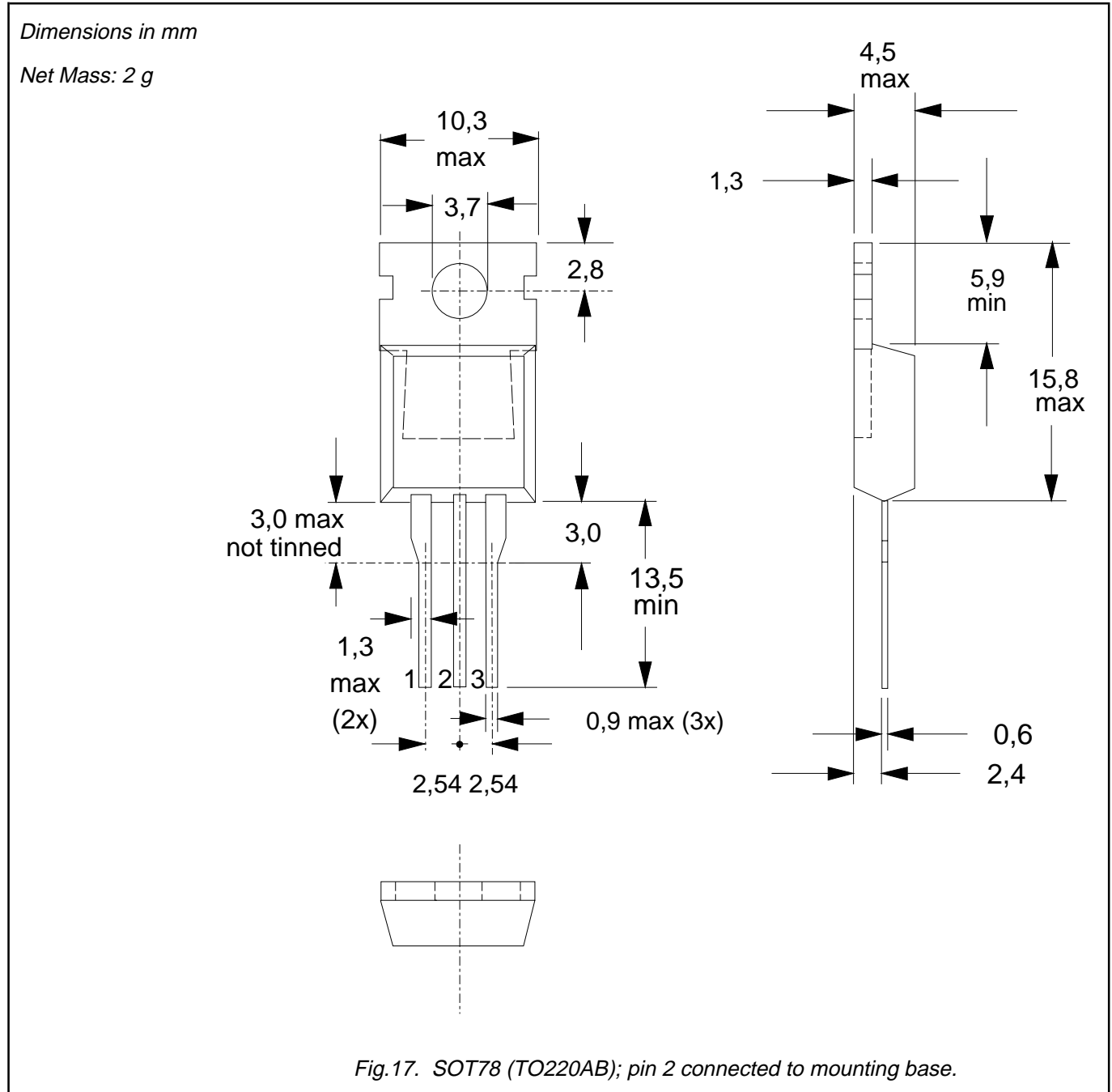
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PHP60N06LT, PHB60N06LT

**MECHANICAL DATA**



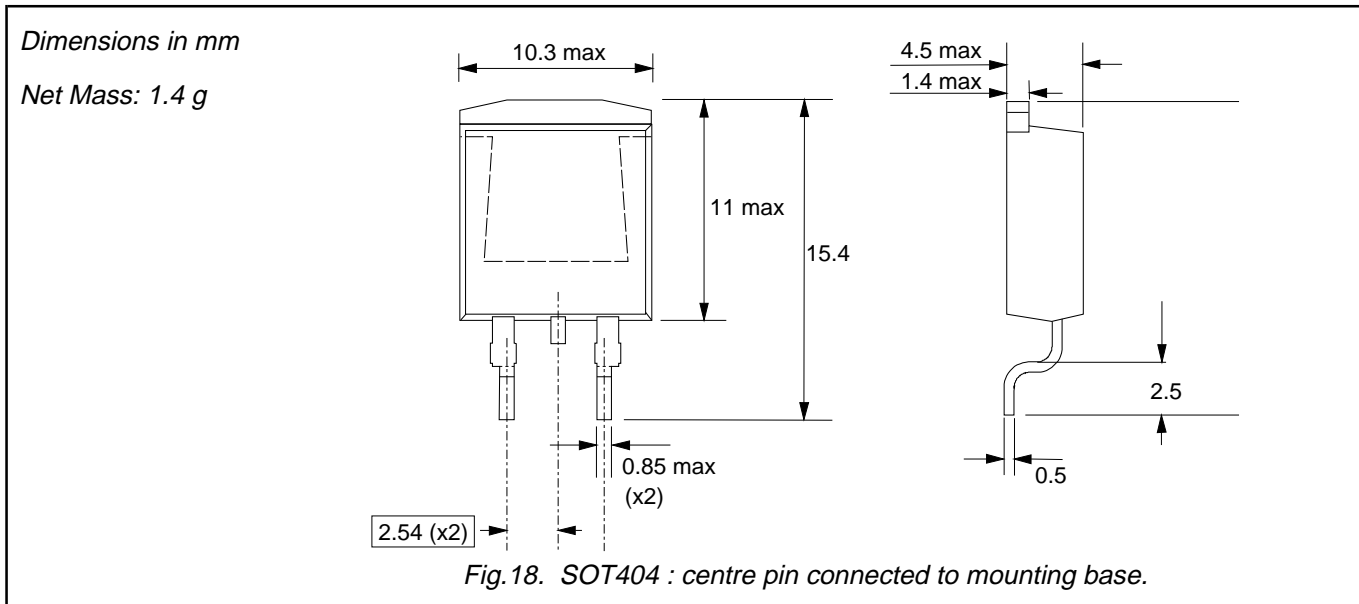
**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Refer to mounting instructions for SOT78 (TO220) envelopes.
3. Epoxy meets UL94 V0 at 1/8".

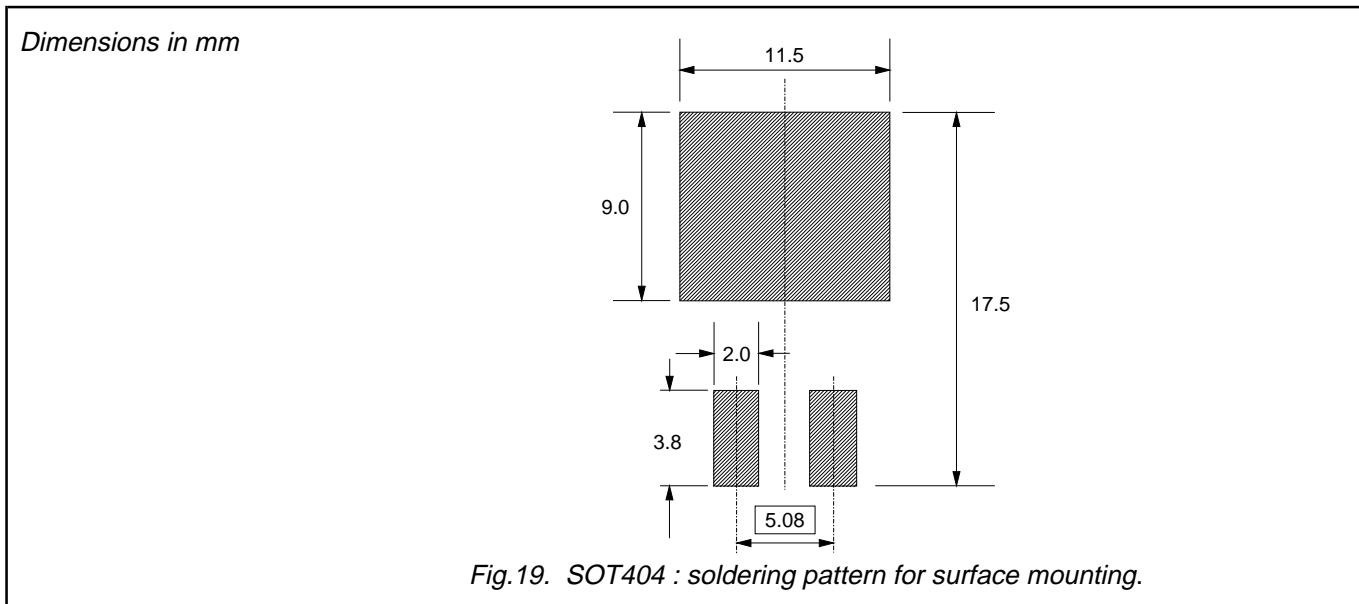
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**MECHANICAL DATA**



**MOUNTING INSTRUCTIONS**



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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	
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